Investigation of a Parallel Resistorless ADC

Maria Stanoeva, Angel Popov

Abstract: *A parallel resistorless analog-to-digital converter (ADC) architecture based on CMOS inverters used as comparators is investigated. Its advantages are the fully digital structure, the lack of resistor ladder and the asynchronous mode of operation, which diminishes both area and power and makes it suitable for system-on-chip solutions. The ADC is made of so-called "threshold inverter comparators" (TIC) with built-in threshold voltage which depends on the ratio of transistor areas. A method for an automatic determination of the sizes of the N-channel and P-channel MOS transistors is proposed. The static and dynamic behavior of the ADC is studied. Recommendations for future investigation are given.*

Key words: *parallel resistorless ADC, threshold inverter comparator, mixed-signal design.*

INTRODUCTION

The bursting development of mixed-signal system-on-chip (SOC) applications leads to a growing need of more sophisticated in terms of speed, area, noise immunity, etc., circuit designs. This is particularly important in analog-to-digital converter (ADC) design, which is often the bottleneck in the design of SOC solutions. The flash architectures constructed of latched comparators are preferred for their speed and inherent monotonicity, but they have large area and power dissipation. In addition, the latched comparators cause substantial noises on the input signal (kickback noise [4]) and on the supply voltage lines. The present work investigates the features of an asynchronous resistorless threshold inverter comparator (TIC) ADC. It is organized as follows: a brief overview of the problem is presented, the method for comparator threshold voltage V_{THI} is presented, an example is given and its static and dynamic characteristics are discussed.

An asynchronous ADC based on CMOS inverters (Fig. 1) was proposed in [2]. Stages with the so-called "dynamic hysteresis" [1, 3] are connected after the comparators. They are Schmitt triggers with time controllable noise immunity, that is, with a single threshold voltage, so that they do not degrade comparison accuracy. The operation of the ADC is asynchronous, i.e. the switching of the 2^n comparators is more or less uniformly distributed with respect to the input signal. Thus the noises on the power supply lines are reduced and the total power consumption compared to the pure flash ADC may be diminished from 2 to 5 times depending on the input signal shape.

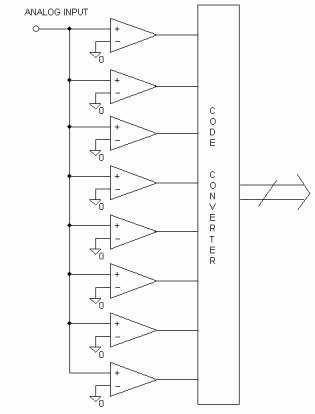

Figure 1. Parallel resistorless ADC based on TIC

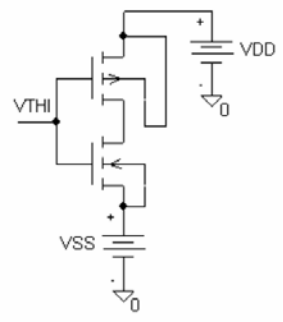

Figure 2. CMOS inverter used as TIC

In [7] a similar architecture is proposed. It consists of two cascaded threshold inverter comparators and a gain boosting stage. The comparator threshold voltages V_{THI} are obtained by simulation. In standard 0.25μ CMOS technology the authors obtain an operation speed of 1 GSPS.

In a previous work [5] a method for an automatic determination of the comparator threshold voltages is given. The results have shown that the analytical solution proposed in [6], which holds when both transistors operate in the pentode area of their characteristic, neglects the short-channel effect and cannot be applied for the existing CMOS technology. Some aspects of ADC dynamic behavior were discussed.

THRESHOLD VOLTAGE DETERMINATION

The analytical solution (1) for the comparator threshold voltage VTHI is given in [6],

$$\sqrt{\frac{\beta_P}{\beta_N}} = \frac{|V_{SS}| + V_{THI} - V_{TN}}{V_{DD} - V_{THI} - |V_{TP}|} \tag{1}$$

where β_N and β_P are transistor gain factors, V_{TN} and V_{TP} are the threshold voltages of the N-channel and P-channel MOS transistors, V_{SS} is the voltage at the source of the NMOS and V_{DD} is the voltage at the drain of the PMOS transistor (Fig. 2). A *PSpice* simulation was used instead and an experimental curve was obtained for the comparator threshold voltage V_{THI}. The parameter *k* (2) was used to obtain the dependence of V_{THI} on different transistor area ratios.

$$k = \frac{W_P / L_P}{W_N / L_N} \tag{2}$$

The values of comparator parameters are as follows: V_{SS} = 0V, V_{DD} = 2.5V, k = 0.45÷20, and W_N/L_N = const. The resulting characteristic is given in Fig. 3

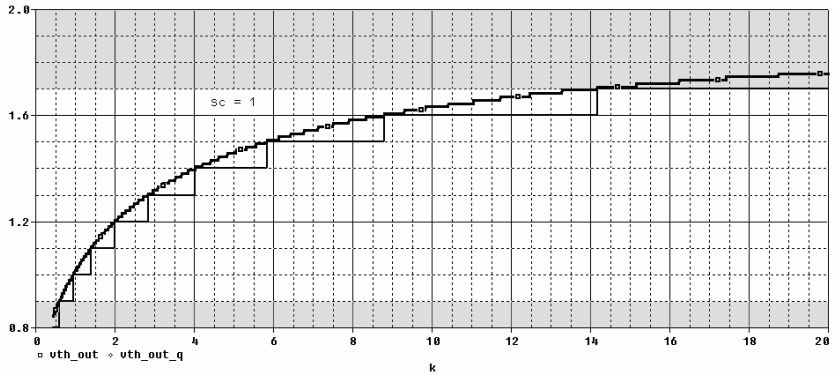

Figure 3. Inverter threshold voltage V_{THI} as a function of transistor area ratio *k*

The non-shaded area of the plot corresponds to the chosen range of 0.8V for V_{THI}. A *PSpice* macro was used to construct the step function, from which the values of transistor area ratio *k* for a chosen level of quantization were determined. The procedure can be easily adapted to different transistor models, input voltage full-scale range and ADC resolution.

ADC INVESTIGATON

The method of area size determination was applied for a LEVEL7 0.18μ CMOS technology with minimum square size of 0.44μ. As an example a 3-bit ADC was simulated and eight values of *k* were determined (Table 1).

Table1. Transistor area ratio

V_{THI}, V	k	P□/N□
1	0.91	0.44 / 0.48
1.1	1.4	0.62 / 0.44
1.2	2.02	0.89 / 0.44
1.3	2.95	1.30 / 0.44
1.4	4.26	1.87 / 0.44
1.5	6.33	2.79 / 0.44

Table1. Transistor area ratio		
V_{THI}, V	k	P□/N□
1.6	9.87	4.30 / 0.44
1.7	16.2	7.13 / 0.44

The area of the top-most comparator does not follow its resolution by an exponential law, but depends rather on the input voltage full-scale range. For instance, for V_{FSR} = 800 mV, k_{max} = 16.2, regardless of the chosen ADC resolution.

Transfer characteristics

The values of the threshold voltages V_{THI} were recorded at the point of the transfer characteristic where the input voltage of the inverter equals its output voltage. A grid of equally spaced characteristics was obtained. Afterwards, as in [7], a stage of two cascaded inverters was used to increase the gain and to sharpen the transfer characteristic (Fig. 4). The transistor area ratio *k* of the inverters in the second stage was chosen ~ 2.4 to obtain optimal values for V_{TH2nd} ~ ½ V_{DD} and approximately equal rising and falling edge delays. The threshold voltage displacement caused by the second inverter is shown in Fig. 5. It can be seen that the error is less than 3% and the influence of the buffer inverter size is negligible.

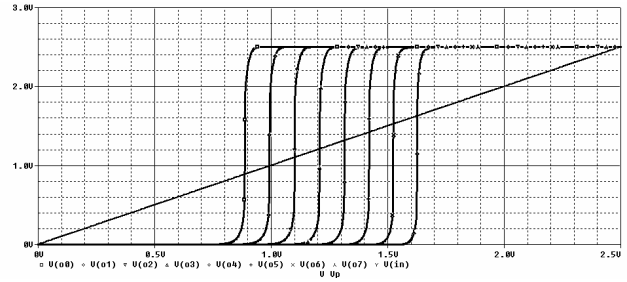

Figure 4. Threshold voltage grid for a 3-bit ADC with two cascaded inverters

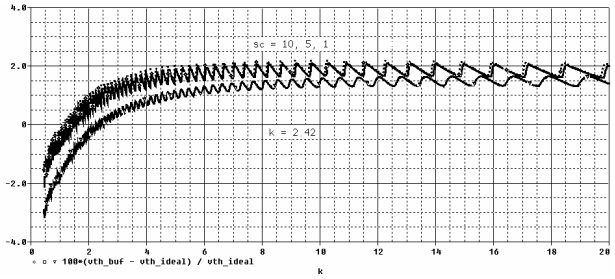

Figure 5. Threshold voltage error after the second inverter as a function of scaling factor *sc*, in %

Dynamic behavior

The time-domain analysis shows that the proposed ADC may operate at speeds up to approximately 0.3 GHz without missing code.

The inverter delays for each bit of the ADC have been investigated (Fig. 6). It is seen that the rising edge delay is constant, because of the constant size of the NMOS transistor, while the falling edge delay depends strongly on the increasing size of the PMOS transistor and is dominant for the overall dynamic behavior of the inverter for larger *k*. The second stage inverters were scaled and their static and dynamic behavior was studied. Their delay increases with their scaling factor *sc*. A trade-off between speed and inverter gain has to be made. The experiments have shown that for scaling factors > 5 the delay of the inverter stage reaches ~0.5 ns, the overall operation speed of the ADC degrades quickly and some distortions in comparator threshold voltages V_{THI} occur.

A scaling factor of 2 was chosen for the second stage inverters. Their delay with respect to the input capacitance of the decoding stage is given in Fig. 7.

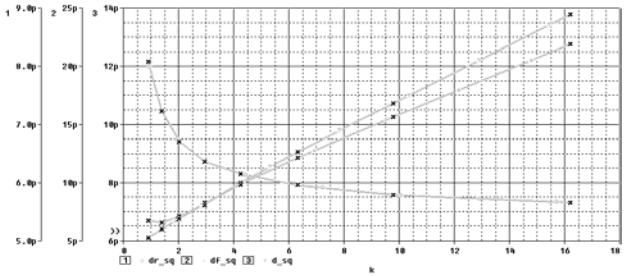

Figure 6. Rising (lower) and falling (middle) edge

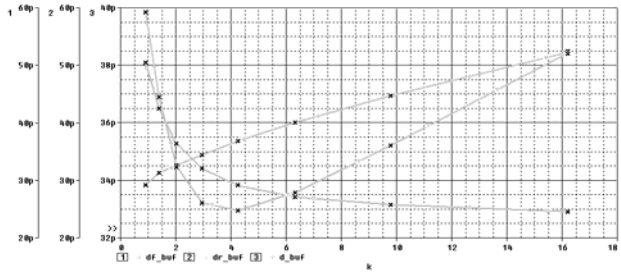

Figure 7. Rising (upper) and falling (lower) edge

delays and average value (upper) of the TIC for the chosen values of transistor area ratio *k* (marked with **x**)

delays and average value (middle) of cascaded inverters for the chosen values of transistor area ratio *k* (marked with **x**)

In Fig. 8 and Fig. 9 the output of the ADC in thermometer code and code 1-of-n is given.

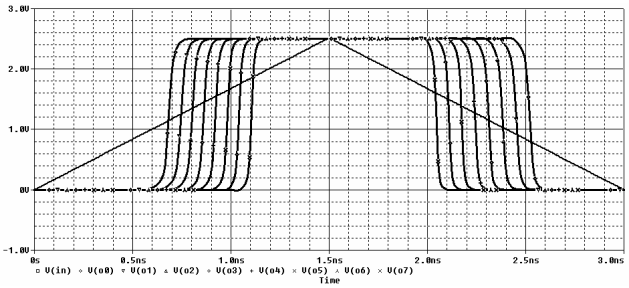

Figure 8. Comparator output in thermometer code

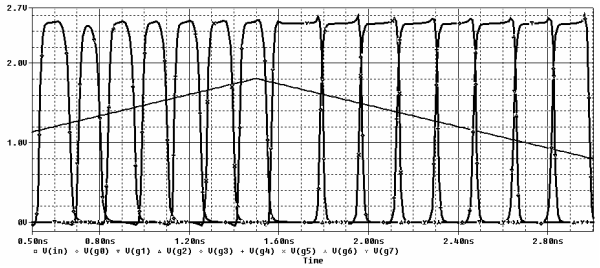

Figure 9. Comparator output in code 1-of-n

It can be seen that the delays of the 1-of-n code on the rising edge of the input signal are larger than the ones on the falling edge (Fig. 10). In Fig. 11 the active time period of the pulse of each bit of the 1-of-n code is shown.

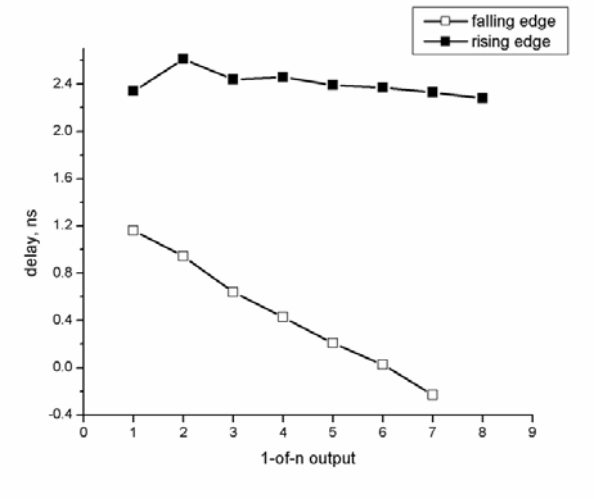

Figure 10. Rising and falling edge delays for each bit of the 1-of-n code generator

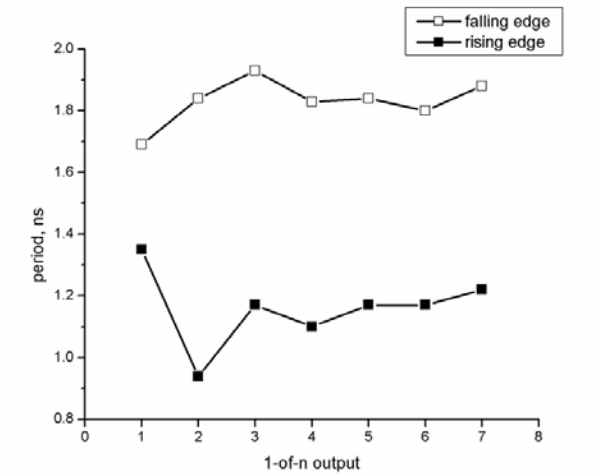

Figure 11. Active time of the pulse of the 1-of-n code generator

The differences in the delays of the top-most and the bottom-most bit of the ADC will become more significant with the increasing of its resolution. An effort has to be made for minimizing these delays, which may lead to some undesired effects during the subsequent code conversion and digital output generation.

CONCLUSIONS AND FUTURE WORK

Some aspects of the design of a high-speed parallel resistorless ADC based on CMOS threshold inverter comparators were investigated. The design is based on a previously proposed procedure for automated determining of transistor area ratios *k* for a given resolution. The static and dynamic behavior of the ADC was explored. The implemented example proves the feasibility and the benefits of such a structure. The standard CMOS technology design is simple and suitable for SOC applications, with smaller size and power consumption.

The results obtained so far provide the grounds for making the following conclusions and outlining the trends for future research:

- As it was expected the delays of the different comparator stages are different. For higher frequencies this may cause missing codes. More profound investigation must

be performed for equalizing the delays without degrading the accuracy of comparator threshold levels.
- An optimal solution for subsequent code conversion and synchronization of the ADC has to be elaborated.
- The influence of the technological process variation as well as the truncation or rounding of transistor area ratio *k* needs more comprehensive investigation.
- A drawback of the comparator is that the input is not differential. This can be mitigated by a differential amplifier at the ADC input.
- To increase the noise immunity and neutralize any ringing noise on the input line without degrading comparison accuracy, a stage with time controllable noise immunity (Schmitt trigger with dynamic hysteresis) may be added to the design.

REFERENCES

[1] G. Panov, D. Manova, A. Popov, "Comparator with dynamic hysteresis", Electronics Letters, 2nd September 1999, Vol. 35, No. 18, pp. 1497-1498.

[2] A. Popov, D. Manova, "A parallel resistorless CMOS ADC", proc. of 6th International Scientific and Applied Science Conference ELECTRONICS'97, book 1, pp. 204-209, September 1997, Sozopol, Bulgaria.

[3] A. Popov, D. Manova, G. Panov, "Asynchronous Comparator Circuits for Parallel Analog-to-Digital Converters", Proc. of the IXth Int. Symp. on Systems Theory, Robotics, Computers & Process Informatics - SINTES 9, June 4-6, 1998, Craiova, Romania, vol.III, pp. 153-160.

[4] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.

[5] M. Stanoeva, A. Popov, "Some Problems in the Design of Parallel ADC Based on Threshold Inverter Comparators", given for reviewing at IEEE Workshop on Signal Processing Systems (SIPS'05), Athens.

[6] N. H. E. Weste, K. Eshraghain, Principles of CMOS VLSI design. A system's perspective, 2nd ed., Addison-Wesley Pub. Comp., 1993.

[7] J. Yoo, K. Choi, A. Tangel, "A 1-GSPS CMOS flash A/D converter for system-on-chip applications", IEEE Computer Society Workshop on VLSI, pp. 135-139, April 2001.

ABOUT THE AUTHORS

Ms. Eng. Maria Stanoeva, is a PhD student in the Department of Computer Systems, Technical University of Sofia, E-mail: mstanoeva@yahoo.com

Assoc. Prof. Angel Popov, PhD, Department of Computer Systems, Technical University of Sofia, E-mail: anp@tu-sofia.bg